

Two-stage synchronizer for START and STOP pulses

FDC = asynchronous clear

Start pulse

Stop pulse

CLK

RESET

Global Reset

Timer count enabled when START and not STOP

16 bit counter, async clear

START\_S1B

START\_S2B

START\_S3B

STOP\_S1B

STOP\_S3B

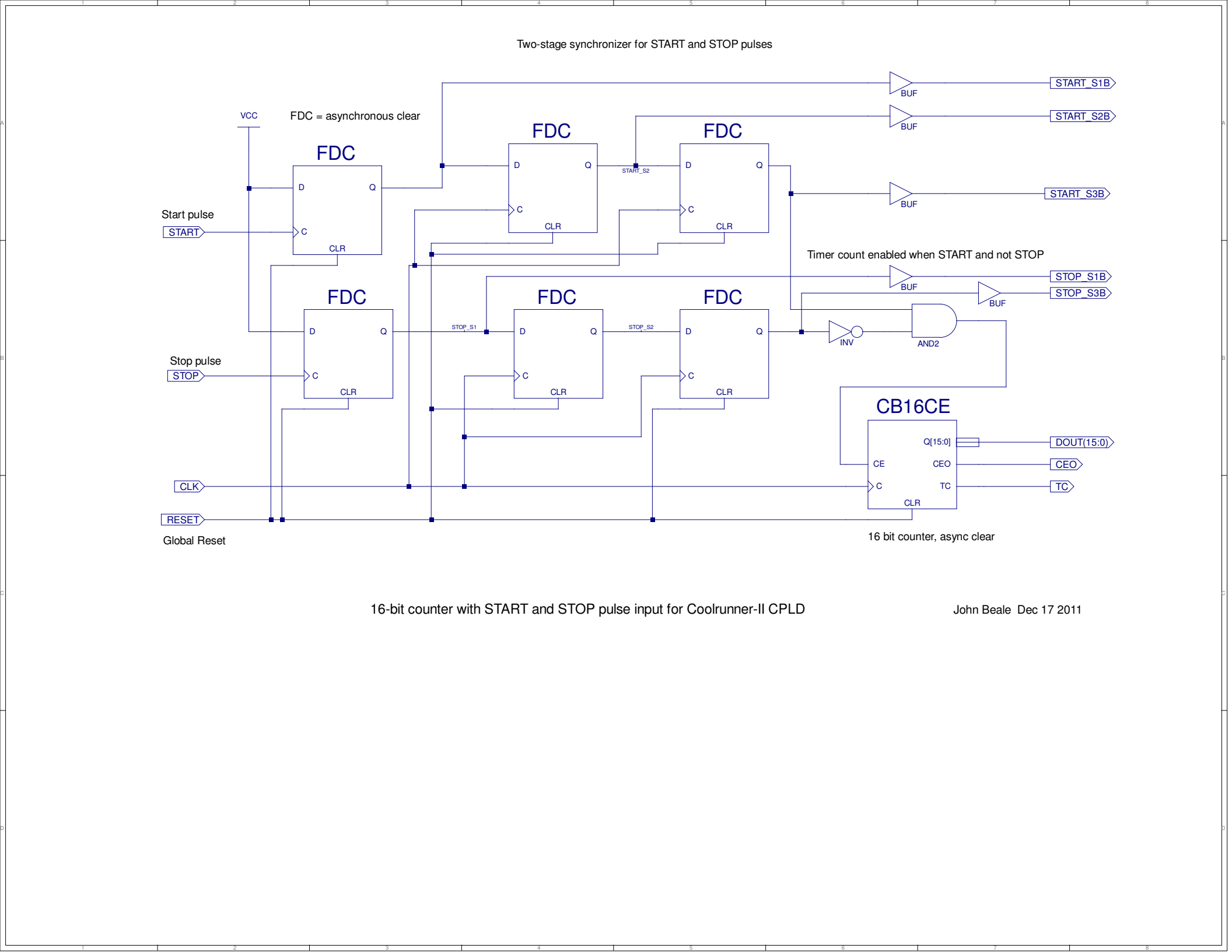
DOUT(15:0)

CEO

TC

16-bit counter with START and STOP pulse input for Coolrunner-II CPLD

John Beale Dec 17 2011



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